PROCESSOR ARCHITECTURE FOR COMPRESSION AND DECOMPRESSION OF VIDEO AND IMAGES

ABSTRACT OF THE DISCLOSURE

A video encoder/decoder includes a vector pipeline unit and is configured only once by a processor to encode/decode data in accordance with any one of the JPEG, MPEG1, MPEG2 or MPEG4, H.261 or H.263 compression standards. The configuration data is stored in a configuration register of the video encoder/decoder. An optional ROM stores the configuration data for subsequent reading and loading--by the processor--into the configuration register. The vector pipeline unit includes: a run-length decoder, a binary arithmetic logic unit , a binary multiplier/divider, an accumulator, a barrel shifter, a round/modify unit, a saturate logic unit, a status register and a run-length encoder. Each component of the vector pipeline unit is optionally enabled or disabled. By disabling one or more components of the vector pipeline unit the power consumed by the encoder/decoder is reduced. The vector pipeline, after being configured continuously encodes/decodes vectors of data according to the configured standard, without requiring any additional configuration or software programming. The status register gathers statistical data on the saturated data and supplies the statistical data to the processor, thereby, further improving the performance of the video encode/decoder. The video encoder/decoder encodes/decodes data based on any other compression standard with additional configuration or software programming.

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